REMARKS

In response to the Office Action mailed November 30, 2004, Applicants amend their application and request reconsideration. No claims are added or cancelled so that claims 1-4 remain pending.

The invention is directed to an integrated circuit that, in the circuit defined by claim 1, includes a semiconductor amplification element, which is a transistor in the illustrated embodiments of the invention, and a bias circuit. The semiconductor amplification element receives a power source voltage at the terminal 7 in the illustrated embodiments. The bias circuit receives a power supply voltage from a different power source, at a terminal 6 in the illustrated embodiments. As explained in the patent application, the first voltage supplied to the terminal 7 of the illustrated embodiment is changed depending upon whether the semiconductor amplification element is producing a high power output or a low power output. The two power sources, one for the semiconductor amplification element and one for the bias circuit, are independent but are interconnected. In the embodiments of Figures 1 and 3, the terminal 6 is connected to the terminal 7 through two transistors, Q4 and Q5, as well as a resistor R3. In the embodiment of Figure 2, that interconnection occurs through two diodes, D1 and D2, and a resistor R4.

Claim 1 has been amended in accordance with the disclosure of the patent application as well as the illustrated embodiments to explain that different power sources supply different voltages to the semiconductor amplification element and to the bias circuit.

Claim 2 was rejected as indefinite on the grounds that no figure showed the interconnection of the first and second power sources through a semiconductor element that is a transistor. According to the Office Action, the interconnection is through the resistor 10 in the embodiments of Figures 1 and 3. Of course, there is an interconnection through that resistor 10 but the interconnection must also pass through at least the transistor Q5. Thus, the figures of the patent application as well as the disclosure provide more than adequate support for claim 2. The rejection of claim 2, upon reconsideration, should be withdrawn.

Claim 1 was rejected as anticipated by Baro (U.S. Patent 3,896,394) and claims 2 and 3 were rejected as obvious over Baro considered by itself. These rejections are respectfully traversed.

It is sufficient in response to the rejection to point out that there is only a single power supply voltage in the circuit of the single figure of Baro. That single power supply is represented by the line providing a voltage V_0. While the transistor Q2 in Baro certainly provides a bias voltage to the semiconductor amplification element represented by the transistor Q3, there is no independence of power supply voltages supplied to those two

transistors because there is only a single power source providing a single voltage. This difference prevents not only anticipation of claim 1 but also the rejection for obviousness of claims 2 and 3, a rejection that depends for its propriety on the rejection for anticipation of claim 1. Accordingly, upon reconsideration, these rejections should be withdrawn as to the claims now presented.

Claims 1-4 were rejected as unpatentable over Yamashita (U.S. Patent 6,731,171) in view of Bailey et al. (U.S. Patent 5,654,672, hereinafter Bailey). This rejection is respectfully traversed.

In making the rejection, attention was directed to Figure 2 of Yamashita. It was asserted that all of what is claimed in claim 1 is illustrated in Figure 2 of Yamashita, with the exception of the semiconductor element linking the power source of the semiconductor amplification element 10 and the bias circuit 52. Of course, there is but a single power source in Yamashita, as in Baro, so that the same voltage is supplied to both the biasing transistor 52 and the amplifying transistor 10, as shown in the circuit of Figure 2 of Yamashita.

According to the Office Action, Figure 3 of Bailey shows a bias circuit 22 including a bias transistor 31 connected to a power source via a resistor. There is no disagreement with this characterization of Figure 3 of Bailey. However, Bailey does not describe any interconnection between the power source of the amplification transistor 23A and the power source of the biasing transistor 31 as in the invention defined by claim 1. Therefore, no modification of Yamashita by Bailey could include all of the elements of claim 1 or any of the dependent claims 2-4. Thus, *prima facie* obviousness has not been demonstrated with regard to any claim now presented and this rejection cannot be properly maintained.

Since the foregoing amendment places the application in form for allowance, prompt and favorable action is earnestly solicited.

Respectfully submitted,

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